REMARKS

In the Official Action mailed on **18 February 2010**, the Examiner reviewed claims 1-20. Examiner rejected claims 1-20 under 35 U.S.C. § 103(a) as being unpatentable over Orsic (U.S. Patent No. 4,817,082, hereinafter "Orsic"), in view of Blanc et al. (U.S. Patent No. 6,606,300, hereinafter "Blanc").

Rejections under 35 U.S.C. § 102

Examiner rejected claims 1-20 under 35 U.S.C. § 103 as being obvious based on Orsic in view of Blanc. More specifically, in rejecting the independent claims, Examiner argued as follows:

> [**Orsic**] **does not teach** a transmitter in the plurality of transmitters is coupled with an output of an AND gate, a first input of the AND gate is asserted when the transmitter is allowed to transmit based on the presence of the token, a second input of the AND gate is asserted when the receiver is ready to receive from the transmitter, and the transmitter is allowed to transmit when the output of the AND gate is asserted. However, **Blanc does teach such a limitation**. According to Blanc, a flow control process for a switching system teaches an AND gate that receives inputs, such as a signal associated with the possibility of transmitting a cell and a signal associated with authorizing a positive gate signal, can deliver a positive GRANT signal (see Blanc column 39 lines 25-60). Therefore, it would have been obvious to a person of ordinary skill in the art to have combined Blanc's teaching of an AND gate that receives two input signals and outputs a signal with Orsic's teaching of a logic circuit that receives a signal from a flip-flop indicating the presence of a e-bit stored and a signal from the output controller (receiver) indicating whether its busy or not and then outputs a grant signal to the input controller … because as known an AND gate is a digital logic gate that implements logical conjunction and therefore can be construed as a logic circuit.[1]

1 see office action, pages 5-6, emphasis added

Applicant respectfully disagrees with the rejection. Although describing an AND gate that is used to control the generation of a GRANT signal, Blanc nowhere describes the AND gate or the signals in the claimed embodiments.

Generally, Blanc describes a flow control mechanism that does not require additional control leads or wiring for transporting the different flow control signals for slowing down some components in the switching architecture.[2] In describing the flow control mechanism, Blanc describes "merging circuits" that are coupled between transmit switch core access layers (SCALs) and elementary switch cores to "provide fan-in" from the larger number of SCALs to the smaller number of elementary switch cores:

> Similarly, a second set of sixteen merging circuits 6811-0 to 6811-15 is associated with the sixteen transmit SCALs 6411-0 to 6411-15 **so as to provide a fan-in operation for the four elementary switch cores** 6101, 6111, 6121 and 6131 (composing a second output group).[3]

Each of the merging circuits includes a multi-stage arbiter with a first stage arbiter and a second stage arbiter.[4] The first stage arbiters receive a Queue_empty signal from a pair of the SCALs[5] and generate an intermediate Queue_empty signal that is forwarded to the second stage arbiter.[6] From the received Queue_empty signals, the second stage arbiter generates a GRANT signal that is sent back to the first stage arbiters to be forwarded to a selected switch core to enable the switch core to transmit data.[7] In other words, Blanc's Queue_empty and the GRANT signals are closest to being equivalent to a "**request**" from a switch core to transmit data, and an "**enable**" from the merging circuit that enables a selected switch core to transmit data. As described by Blanc:

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2 see Blanc, col. 1, lines 56-60
3 see *id.*, col. 31-32
4 see *id.*, FIG. 20, elements 7110, a first stage arbiter, and 7130, a second stage arbiter
5 see id., FIG. 20, first stage arbiter 7110 in merging unit 6810 receives busses 7111 and 7112 from switch cores 6100 and 6110, respectively
6 see *id.*, FIG. 20, busses 7131 and 7132 to second stage arbiter 7141
7 see *id.*, col. 35, line 13-col. 36, line 46

> When one among these 8 GRANT control signals is set at a low state, **this entails a disabling of the corresponding [off-chip driver]**. The 8 EVEN Grant control signals are transmitted to the corresponding one among the last 8 drivers composing the set of 16 OCD drivers and, similarly, they are used for disabling the corresponding OCD driver when they are set at a low state.[8]
>
> Each switch core element generates a Queue_Empty control signal which is in phase with its cell cycle in order to indicate whether or not **there is something to transmit** on the next cell cycle.[9]

As can be seen from the description of each of these signals, neither of the signals is a signal that indicates "receiver is ready to receive from the transmitter." Although Blanc describes a third input to AND gate 7320 (which is the only AND gate addressed in the cited section of Blanc) -- the "GATE 7322" input -- Blanc nowhere describes the GATE 7322 input, i.e., Blanc does not provide any detail of the source of the GATE 7322 signal or what the exact purpose of the GATE 7322 signal actually is, aside from enabling the generation of token 7325. Thus Blanc nowhere describes the signals from the claimed embodiments.

In addition to not describing the signals in the claimed embodiments, Blanc nowhere describes an AND gate with the function in the described embodiments. In the Blanc system, AND 7320 is used to **generate the token**:

> As it appears in FIG. 21, when there is an occurrence between the three inputs of the AND gate 7320-j--that is to say that there is simultaneously a request for a GRANT control signal associated with the actual possibility of transmitting a cell to the SCAL element (signal 7141-j) and the AND Gate also being authorized by a positive Gate signal (7322-j)--the AND gate 7320-j can deliver a **positive GRANT control signal or a so-called TOKEN control signal that will be distributed to the first-stage arbiters**.

8 see *id.*, col. 34, lines 1-7
9 see *id.*, col. 38, lines 13-17

The generation of the token in the claimed embodiments occurs in a different portion of the circuit.

In summary, Blanc describes a system with different signals and that does not produce the output signal in the claimed embodiments. Thus, Blanc is fundamentally distinct from the claimed embodiments.

Applicant has amended the independent claims in the instant application to clarify the subject matter in the claimed embodiments. More specifically, to clarify the arrangement and purpose of the inputs to the AND gate in the claimed embodiments. These amendments find support in FIG. 7 and pars. [0060]-[0063] of the instant application.

Because Blanc nowhere describes the AND gate or the signals in the claimed embodiments (and Examiner expressly acknowledges that Orsic does not disclose these things), Blanc in combination with Orsic cannot render the claimed embodiments obvious.[10] Applicant therefore respectfully requests the withdrawal of the rejection under 35 U.S.C. § 103 based on Orsic in view of Blanc.

10 see Manual of Patent Examining Procedure (MPEP) §§ 2141(III) and 2143.01(IV-VI)

CONCLUSION

It is submitted that the application is presently in form for allowance. Such action is respectfully requested.

Respectfully submitted,

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